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The Temperature Effect on the Operating Mode of FeRAM

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Abstract: In this paper, we present the study of Landau's phase. phase transition in the medium dielectric which the FeRAM is working. The existence of two phase (parra-ferroelectric) can be able to explain the phenomenon of reading / writing in the FeRAM.

Keywords: Dielectric; ferroelectric capacitor; FeRam; Landau theory of phase transition

1 Introduction

Ferroelectric random access memories have attracted much attention because of the lower writing voltage and faster switching speed than those of Flash memory [1],[2]. Recently ferroelectric memory field effect transistors (FEMFETs) with a metal-ferroelectric - insulator-silicon (MFIS) gate structure have emerged as promising non volatile memory devices [3]. The superior characteristics of FEMFETs include a single-device structure, small size, low power consumption, and non-destructive readout operation [4]. The purpose of the insulator layer in MFIS structure is to prevent the reaction and inter-diffusion between the ferroelectric layer and silicon substrate that greatly degrades the device characteristics [5],[6]. The low leakage current and good interface property can be expected to be achieved after the insulating material is inserted as a buffer layer. Recently, $BiFeO_3$ has attracted great attention for its multi-ferroic properties including dielectric and coupled ferroelectric and magnetic ordering [7],[8]. Furthermore, low crystallization temperature and large remnant polarization (P_r) of $BiFeO_3(BFO)$ are suitable for non volatile memories in comparison with other ferroelectric materials. The characteristics of the MFIS structures with ferroelectric BFO thin films and ZrO_2, $Ba(Sr,Ti)O_3$, Y_2O_3, and HfO_2 insulating buffer layer on silicon substrates have been reported in these years [9],[10],[11].
In this paper, we study the temperature influence on the behavior of the FeRAM, so we rely on the theory of phase transition,it was used in previous work by Ourrad et al. [2007] and Benouaz et al [2010] see [12],[13]. The material chosen in our study is the Rochelle salt ferroelectric, of chemical formula $CO_2K-2CHOH-CO_2Na,4H_2O$ which changes phase at the critical temperature$Tc = 23.5°C$ [14].

2 Characterization of FeRAM

2.1 Configuration of FeRAM

The Fig.1 shows a schematic drawing of the FeRAM structure [15].

The unit cell was formed by one transistor and one ferroelectric capacitor which were connected in parallel, during the operation, one capacitor was selected randomly by cutting off it's pare transistor.
Controlling the voltage across the capacitor is provided by three conductive lines called "bit line", "word line", "plate line".

2.2 Basic hypothesis of dielectric material

The free energy of a dielectric material may be developing as a function of polarization by [16]:

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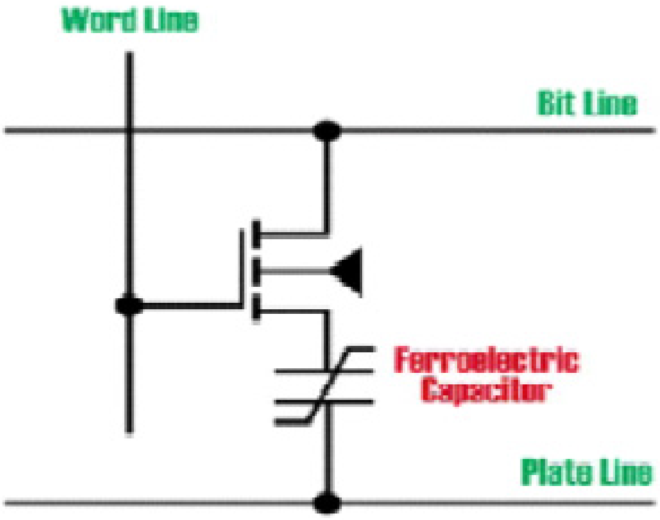

Figure 1: Standard structure 1T/1C, (1 transistor (T) for 1 capacitor (C))

$$G(D,T,E)=\frac{A}{2}D^2+\frac{B}{4}D^4 \tag{1}$$

According to the thermodynamics of dielectrics, we have the following relations [17]

$$E=\left(\frac{dG}{dD}\right) \tag{2}$$

So,

$$E=AD+BD^3 \tag{3}$$

On the other hand, the dielectric permittivity expressing the property of the material to oppose the passage of electric current, is given by equation (4)

$$\varepsilon=\frac{dD}{dE} \tag{4}$$

From equations (3) and (4), we obtain the relation (5) which connects the dielectric permittivity ε to the displacement macroscopic of dipole moment $\overrightarrow{D}$, the form of equation (5) is as follows

$$\frac{1}{\varepsilon}=A+3BD^2 \tag{5}$$

The variation of dielectric permittivity versus electric induction and temperature is nonlinear, and is given by relationship (6)

$$\varepsilon^{-1}=A_0\left(T-T_c\right)+3BD^2 \tag{6}$$

2.3 Modelling FeRam

FeRAM memory chosen in our study is the combination 1T/1C, and to increase performance of non-volatility, we must control the behavior of the capacitor and transistor constituting the memory, for this study we propose two mathematical models, the first represented the behaviour of the ferroelectric capacitor and the second will be for the behavior of the transistor.

2.4 Modeling ferroelectric capacitor

To increase the capacitance, we propose to introduce a ferroelectric material (Rochelle salt) between the anode and the cathode of capacitor [18], its capacity takes the form of equation (7):

$$C = \frac{\varepsilon S}{e} \tag{7}$$

With $\varepsilon = \varepsilon_0 \varepsilon_r$
Applying a voltage on the FeRAM leads to the reorientation of dipole moments according to the relation (8), [19]

$$D = \varepsilon_0 E + P = \varepsilon E \tag{8}$$

With $Q = D.S$
By injecting equation (5) into (7), we obtain

$$C = \frac{S}{e\left(A_0\left(T - T_c + 3BD^2\right)\right)} \tag{9}$$

It can be seen in equation (9); the ability of the ferroelectric capacitor varies in a non-linear with temperature and electric induction.
And to assess the behavior of the ferroelectric capacitor, we can connect it in series with a resistance, the application of Kirchhoff's laws yields the relation (10)

$$RI + \frac{Q}{C} = Ue^{(i\omega t)} \tag{10}$$

With $I = \dfrac{dQ}{dt} = Q^{\cdot}$
Then equation (10) takes the following form

$$D^{\cdot} + \frac{eA}{RS}D + \frac{eB}{RS}D^3 = \frac{U}{R.S}e^{(i\omega t)} \tag{11}$$

2.5 Modeling the transistor

The transistor chosen for our study is MOSFET type (Metal, Oxide, Semi-conductor field effect). The miniaturization of its thickness leads to the birth of a leakage current by tunneling effect; to remedy to this problem, we consider in this work to replace the grid oxide by the ferroelectric material "Rochelle Salt" of higher dielectric permittivity, to have a larger physical thickness for equivalent capacity.
The voltage of the transistor takes the following form equation (12)

$$D_{DS} = \frac{I_{DS}.T_{ox}.L}{\mu^{*}\varepsilon\varepsilon_0\left(U_{GS} - U_{th}\right).Z} \tag{12}$$

With $I_{DS} = \dfrac{dq}{dt}$
The injection of equation (5) in equation (12) yields equation

$$U_{DS} = \frac{T_{ox}.L.S}{\mu^{*}\varepsilon_0\left(U_{GS} - U_{th}\right).Z}\left(A + 3BD^2\right)\frac{dD}{dt} \tag{13}$$

From equation (13), we find that the temporal variation of the induction is nonlinear and because in our circuit the capacitor is connected in parallel with transistor, then we can deduce the relation (14)

$$U_{DS} = \frac{T_{ox}.L.S}{\mu^{*}\varepsilon_0\left(U_{GS} - U_{th}\right).Z}\left(A + 3BD^2\right)\frac{dD}{dt} = \frac{q}{C} = U_0 e^{(i\omega t)} \tag{14}$$

From equation(14), we obtain the relationship of the temporal variation of electric induction versus time

$$\frac{dD}{dt} = \frac{\mu^{*}\varepsilon_0\left(U_{GS} - U_{th}\right).Z.U_0 e^{(i\omega t)}}{T_{ox}.L.S.\left(A + 3BD^2\right)} \tag{15}$$

Equation (15) has the form of an ordinary differential equation, where the electric induction varies in a nonlinear function of temperature versus time.

3 Numerical simulation and results

For numerically solve our differential equations, we use Runge-Kutta's method. First, we plot the variation of the electric induction with the temperature of the ferroelectric capacitor; we based on equation (11)

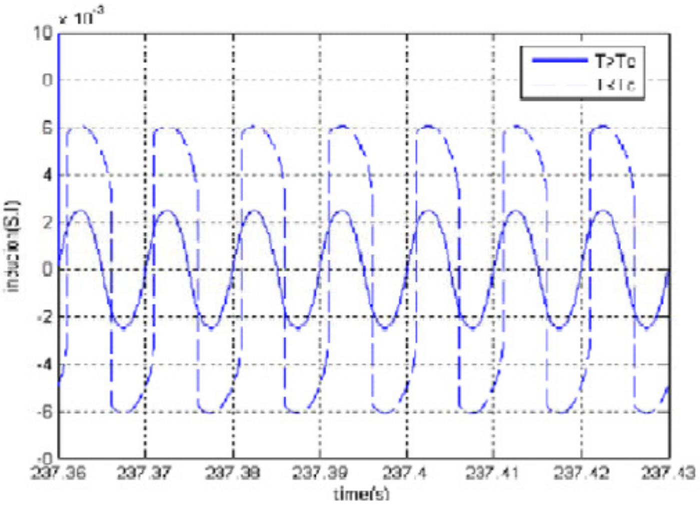

Figure 2: Variation vs. time of the electric induction for T¡Tc and T¿Tc

According to Figure (2), we see that there is a good agreement with the Landau's theory, so in effect for a temperature $T = 22°C < T_C$, the electric induction oscillates towers nonzero, this means in practical terms, that the dipole moment in this phase ferroelectric exist, and can be change its direction under the effect of applying electric field so we can program the FeRAM; but at a temperature $T = 24 > Tc$, the induction oscillates around a zero value, it means the non existence of the electric induction, the capacitor is discharged so we cannot program the FeRAM.
Second, we trace the variation of electric induction of the transistor, while we rely on equation (15).

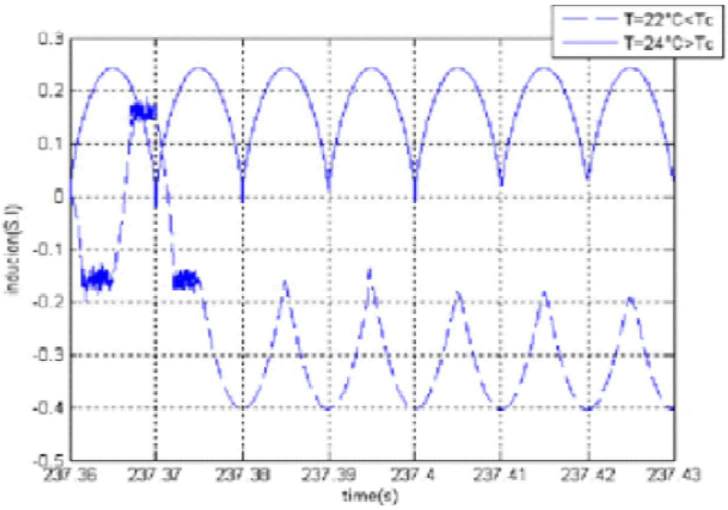

Figure 3: Variation vs. time of the electric induction with temperature and time.

From Figure (3), it is clear that the temperature of phase transition presents a problem since the value of the electric induction change, it goes from a positive value for $T > Tc$ to a negative value for $T < Tc$, thus the principle of writing of the FeRAM binary data "1" and "0" must be verified because the hysteresis loop of this memory will undergo a change

in the remanent polarization.
Third, we trace the variation of the electric induction of FeRAM according to the applied voltage.

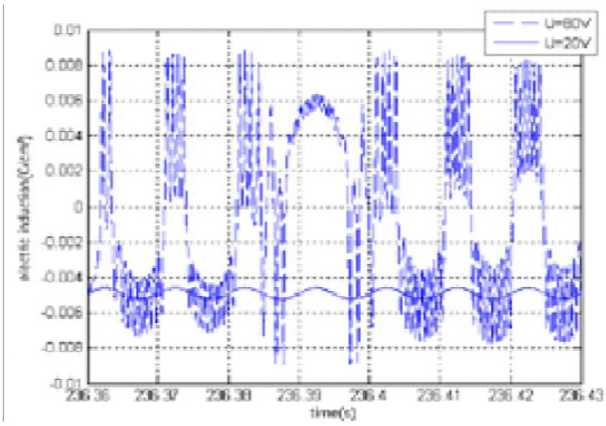

Figure 4: Variation vs. time of the electric induction with voltage.

From figure (4), we note the birth of a strange and unexpected phenomenon in more increases the value of the applied voltage to the FeRAM, the so-called chaotic behavior. But if we observe well this Figure, we note that this behavior is not really chaotic, because at a certain speed, this is called deterministic chaos [20].

4 Conclusion

At the Curie temperature, the Rochelle salt dielectric undergo phase transition, it's include in the FeRAM production increase the efficient of capacitor, but produces a nonlinearity of the electric induction behaviour.
The study of the variation of electric induction versus temperature may lead us to discover a strange phenomenon called "chaos". So we can be able to work around Curie's temperature because beyond this temperature, the electric induction towards zero and the capacitor is discharged, therefore we have problem for the construction of FeRAM.

Nomenclature

$G(P,T,E)$: the free energy of the dielectric
E : the electric field
P : the polarization of the dielectric
T : the temperature
D : the dielectric induction
U : the voltage
T_c : the temperature of Curie
A_0 and B : are two constants which depend on the dielectric medium
ε : the dielectric constant
ε_0 : the permittivity of the vacuum
ε_r : the relative permittivity of the dielectric
e : the thickness of the capacitor
S : the surface of the electrodes of the capacitor

R : the resistance (Ohms)
U_0 : the amplitude of the voltage
U_{DS} : the tension between the drain and the source of the transistor
U_{GS} : the tension between the grille and the source of the transistor
I_{DS} : the intensity between drain terminal and source
V_{th} : the tension of threshold
T_{ox} : Thickness of the gate oxide
q : the electric charge (Cb)
t : the time(s)
μ^* : the mobility of the charge in the Channel
C : the capacitance (Farad)
L : width of the MOS transistor
Z : the width of the grid

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